A Clean Wafer-Scale Chip-Release Process without Dicing Based on Vapor Phase Etching

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Abstract

A new method to release MEMS chips from a wafer without dicing is presented. It can be applied whenever SOI wafers are used that are structured from both the device and the handle side using DRIE. This method enables the release of extremely fragile structures without any mechanical impact on the chips. No more dicing residues or debris are created and deposited onto the wafer. The basic idea consists of etching deep surrounding trenches on the device and the handle layer that are displaced by about 20 µm and thus create overlapping areas. For release, the buried silicon dioxide between the overlapping areas is etched away using hydrofluoric acid vapor phase etching.

1. Introduction

One of the main reasons responsible for the success of MEMS is the fact that the technology and the materials used are quite the same as in microelectronics. On the other side, there are processes commonly used that are not well adapted for the MEMS community. Other than in microelectronics where the mechanical stability of a die almost never leads to problems, MEMS devices show often very fragile mechanical parts like the mass in an accelerometer that's deflection under acceleration is measured or an actuator having small moving parts connected to a spring. This means that MEMS devices are much more critical towards mechanical impact in form of vibration, fluidic flow or sticking. One of the major problems we encountered in the past is related to dicing in order to separate chips from a wafer. Since the dicing is done at the very end of wafer processing, all mechanical structures are laid open. One way of protection consists in embedding the chips in resist prior to dicing. In general this resist layer protects well the fragile structures during dicing but stripping the resist afterwards in acetone and isopropanol is very critical. Dicing debris deposited onto the resist layer during dicing have the tendency to settle down on the silicon surface when the resist is stripped in acetone. This must be avoided since these particles can potentially create short circuits or block moving parts like actuators. In addition, stripping of the resist layer and rinsing is extremely dangerous due to sticking and a big effort has to be done to avoid this.

In this paper we present a novel method of a clean chip release process that can be applied on a wafer-scale and that avoids any dicing and thus the occurrence of dicing debris. The work was carried out within a project where a tilting platform with vertical comb drives was realized. The device was based on SOI technology and implied a deep reactive ion etching (DRIE) on both the device and the handle layer of the SOI wafer. The chip release process was directly integrated in the two DRIE steps. It consists of a rim that surrounds the device and thus defines the footprint of the chip. Such a rim is etched on the frontside as well as on the backside of an SOI wafer. In order to prevent chips breaking off during DRIE, two overlapping zones are created that attach the chip to a remaining grid via the buried oxide. For release, the oxide is etched away using a hydrofluoric acid (HF) vapor phase etching (VPE) system. This topic will be discussed later on.

2. Design Considerations

The basic idea of the new release process consists in etching out the chips when patterning the device. The chips edges are defined by surrounding trenches on either side of the wafer that encompass the devices. To increase wafer stability, the chips are arranged in a manner that a silicon grid of several hundreds of microns width is formed between the chips. The chips are attached to this grid at two opposite corners by overlapping areas of the backside layer and a retaining area connected to the frontside grid. To release the chips from the wafer, the buried oxide beneath the two retaining areas has to be etched away. The retaining areas measure each about 600 x 800 μm^2. They are perforated by a regular pattern of holes arranged in a hexagonal shape. The holes measure 20µm in diameter and serve the HF vapor to access the oxide. The spacing between the holes defines the underetching distance to release the chips. For homogenous DRIE results it is important that the hole diameter does not change over the wafer but instead the spacing between the holes can be varied. By defining zones with different hole spacings, a multi stage release process is possible too and has successfully been tested.

In the DRIE system used here, the wafer is electrostatically clamped onto a helium cooled metal chuck when etched. The cooling is provided by helium flowing in open circular channels embedded in the chuck and covered by the wafer. The pressure of the helium onto the wafer prohibits trenches of the frontside and the backside to coincide since the thin oxide membrane would not withstand the helium pressure. For this reason, the surrounding trenches on either side of the wafer are displaced by about 20 µm toward each other thus preventing any freestanding oxide membrane. The helium pressure exerted on the wafer is also the reason why this chip release method is only applicable for SOI wafers.

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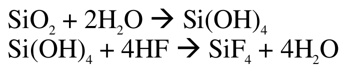
3. VAPOR PHASE ETCHING

The key process in the proposed chip release method is the underetching of the buried oxide in between the overlapping areas using hydrofluoric acid (HF) vapor phase etching. The use of a hydrofluoric acid (HF) vapor phase etching (VPE) system [1]-[4] enables the removal of silicon dioxide in a vaporous environment rather than in an aqueous solution. This is of particular interest since one of the main problems referred to as sticking can be avoided. Sticking is often an irreversible and destructive phenomenon that occurs whenever liquids evaporate and by means of surface tension pull down moveable structures to the substrate until they are in contact. When oxide is etched in aqueous HF, rinsing in deionized water must follow to remove contaminants. Unfortunately water shows a very high surface tension. Several methods have been reported that aim to reduce surface tension or to avoid the transition from liquid to gaseous state of aggregation, i.e. by sublimation. An isopropanol and cyclohexane treatment has to be done followed by a dry freeze step.

First experiments on vapor phase etching were carried out by Holmes & Snell [5] in 1966. They observed that silicon dioxide on a wafer is etched with a comparable etch rate even when the wafer is not in the etch bath but close to. Helms & Deal [3] established that the role of water is to provide a condensed solvent medium for the HF on the surface. Offenberg *et al.* [6] proposed a two step reaction where first the oxide surface is opened by formation of silanol groups by adsorbed H_2O. Subsequently silanol groups are attacked by the HF:



$$SiO_2 + 2H_2O \rightarrow Si(OH)_4$$
$$Si(OH)_4 + 4HF \rightarrow SiF_4 + 4H_2O$$

The above formula shows that water acts as initiator of the etching process as well as reactant. This fact suggests that the etching process can be temperature controlled to maintain in equilibrium the amount of H_2O needed to initiate the process and the amount of reactant H_2O. Indeed the etch rate of silicon dioxide in HF vaporous environment depends strongly on the wafer temperature. Below 30°C we observed condensation, above 40°C no etching toke place at all. Within this temperature window the etch rate can accurately be temperature controlled.

4. SETUP

The setup consists of a Teflon chuck onto which a Kapton heating foil and a temperature sensor is glued. A heat sink in form of a 4-inch plate of stainless steel on top of the heating foil enhances the temperature homogeneity and seals the heating system. The wafer to be etched is loaded onto a dummy wafer on top of the stainless steel plate and fixed with a Teflon ring that is screwed onto the chuck. Then the whole setup is put upside down onto a beaker containing 50% of HF in aqueous solution. A feedback system enables to maintain a stable temperature during the entire process.

Fig. 1: Our Teflon chuck with a clamped wafer and the cables for the heating foil and the temperature sensor.

Fig.2: The frontside and the backside layer of the chip with the corresponding trenches to cut the chips out. The trenches are slightly displaced in order to better withstand the gas pressure of the cooling mechanism during DRIE. The overlapping areas keep the chips in place. To release them, the buried oxide has to be removed.

5. EXAMPLE: TILTING PLATFORM

In this section the three-stage release process is discussed. It was developed for a tilting platform decribed earlier [7]. The tilting platform (Fig. 5b) measures 2 x 2 mm^2 and is intended to tilt an optical resonant grating filter presented in [8] by ± 4° that will be glued onto the platform. Peak tuning of the reflected wavelength is achieved by changing the angle of incidence. Since the device should be used in transmission mode too, the platform had to be equipped with a hole, i.e. a big silicon block had to be released. The original release in BHF destroyed the torsion beams where the platform is attached to due to fluidic flow.

The three stage HF VPE release process is shown in Figure 4. When exposed to vaporous HF, first the SiO_2 beneath the platform is etched away since the through holes in this zone (zone I) are much closer than the ones in the other zones and hence the underetching distance is smaller. By releasing first the platform, we avoid that at any time the silicon block (hatched surface) exerts its weight onto the fragile torsion beams attached to the platform. Instead, the silicon block is attached via the SiO_2 bridge to the frame which is much more stable. Continued etching removes this SiO_2 bridge too and the complete silicon block falls out. At this time, the chip is still attached to the wafer grid since the underetching distance between the holes of the corresponding zone III is larger than the distance between the holes of zone II. After further etching, finally the SiO_2 bridge between the holes of zone III are removed and the chip is released. The Teflon ring that clamped the wafer to the dummy wafer and the metal plate during etching can now be removed as well as the remaining wafergrid. The released chips are now upside down on the dummy wafer and ready to be unloaded.

In the current design we use X-shaped torsion beams that showed an increased stability towards lateral movement. Hence rotation in the xy plane could be supressed by a factor of 20 compared to a straight torsion beam.

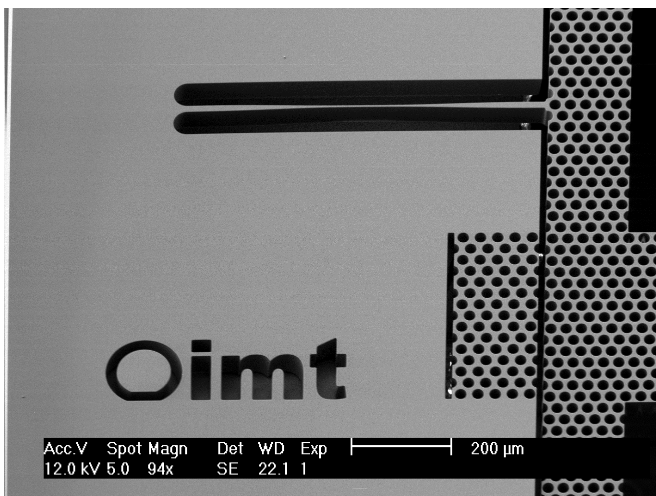


Fig. 3: The tilting platform with X-shaped torsion beams to supress lateral instability.

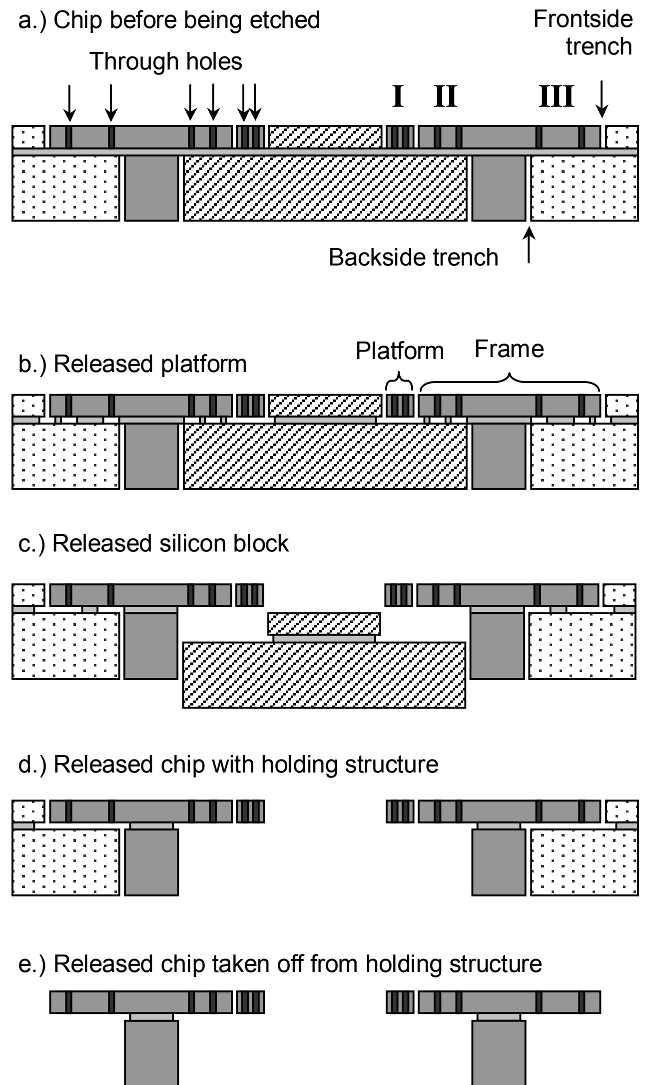


Fig. 4: Shematic sideview of the device on a SOI wafer. The chip itself is given in dark grey, the inner silicon block to be released is presented by the hatched surface, and the wafer grid that keps the chip in place is given by the dotted surface. The troughholes in the zones denoted I, II, and III, respectively, have a different spacing.

a.) HF vapor penetrates through the holes to etch the buried silicon oxide.

b.) The platform is entirely released. The whole weight of the big silicon block (hatched surface) is supported via the oxide bridge to the frame.

c.) The oxide under the frame is etched away and the whole silicon block (hatched surface) is released and falls out. The chip itself is still connected to the wafer grid (dotted surface) via the SiO_2 bridge.

d.) The released chip still in holding structure.

e.) The released chip taken off from holding structur.

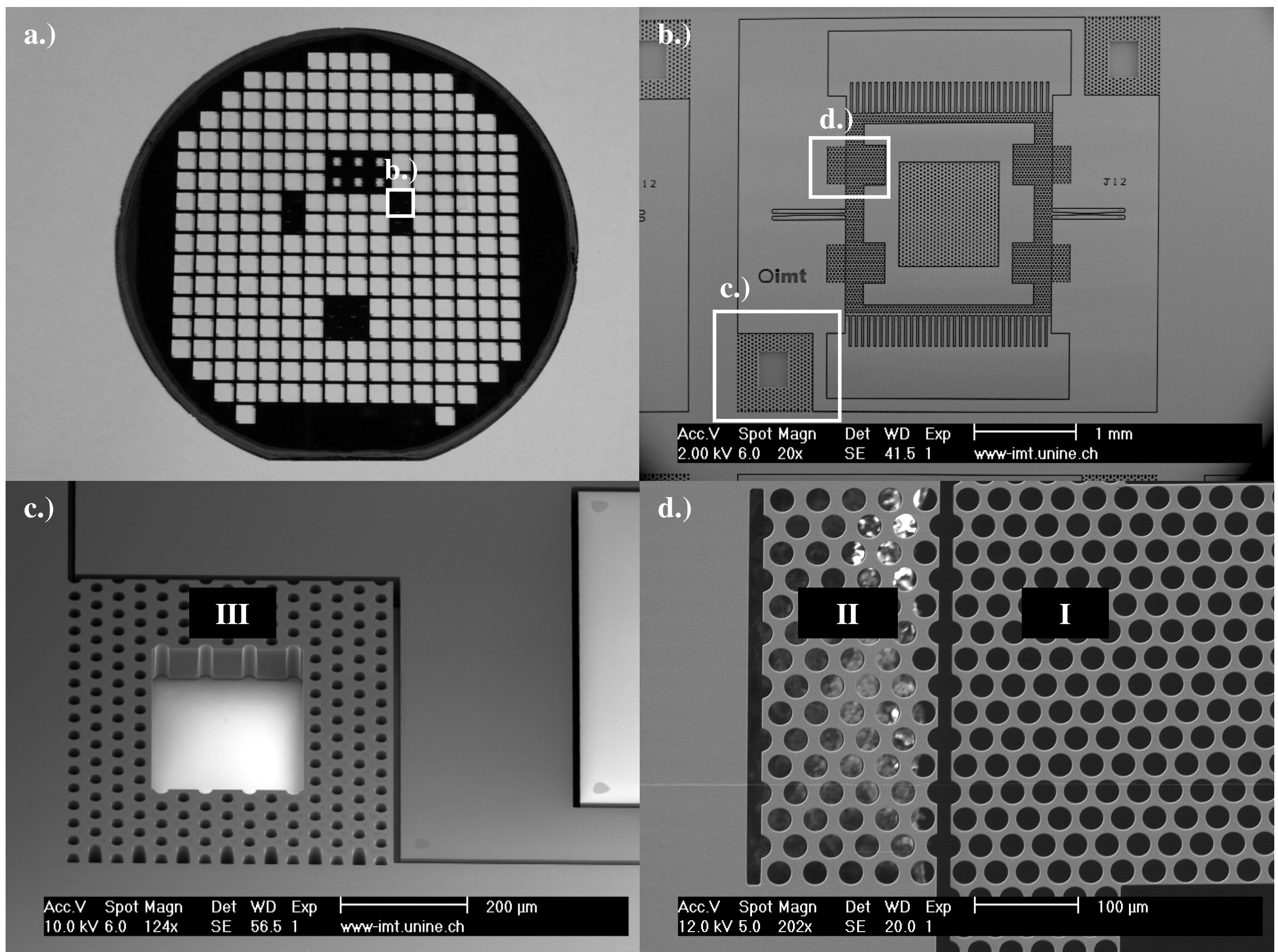


Fig. 5: a.) Remaining waferframe after the chip release. Some chips are left for demonstration.
b.) Section of a.): A chip with surrounding wafergrid that keeps the chip in place.
c.) Section of b.): Holding structure that keeps the chip on the wafer. Hole spacing referred to as zone III in Fig. 4a.
d.) Section of b.): The Si block is first released from the platform (zone I) , but still connected to the frame (zone II).

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